Intel® 31154 133 MHz Bridge

Design Checklist

February 2004

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Contents

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Revision History

Date	Revision	Description
February 2004	001	Initial release

1.0 Introduction

This document highlights design considerations you must review prior to manufacturing an adapter card or motherboard that implements the Intel® 31154 133 MHz Bridge (hereafter “31154” or “31154 Bridge”).

The checklists address important connections to the 31154 Bridge and any critical supporting circuitry. However, the checklists are only for reference; for complete design instructions, refer to the *Intel® 31154 133 MHz Bridge Design Guide* (278944). These checklists are not necessarily complete and do not guarantee proper function of a design.

2.0 Implementation Notes

The following notes are referenced in the checklists in Section 3.0.

Use the recommended values given here unless specified otherwise in the *Intel® 31154 133 MHz Bridge Design Guide* (278944).

Note 1 The recommended value for pull-up resistors for PCI applications is 5.6 KΩ (note that the minimum value for PCI 3.3 V signaling R_{MIN} = 2.42 KΩ, R_{TYP} = 8.2 KΩ, as per the *PCI Local Bus Specification*, revision 2.3, section 4.3.3).

Note 2 The recommended value for pull-up resistors for PCI-X applications is 8.2 KΩ. For PCI-X the minimum pull-up resistor value is 5 KΩ, as per the *PCI-X Addendum to the PCI Local Bus Specification*, revision 1.0b, section 9.7.

Note 3 For plug-in card implementations, the pull-up must be on the motherboard.

Note 4 Connect PVIO and SVIO pull-up resistors to 5 V or 3.3 V power supply through an external resistor—25 Ω (5 V) or 0 Ω (3.3 V), depending on the signaling level of the Primary/Secondary PCI Bus. Refer to the power-sequencing guidelines in Section 6.2 of the *Intel® 31154 133 MHz Bridge Design Guide* (278944).

Note 5 Bypass capacitor recommendations are given in Table 1. Please also note the following:

1. Polymerized organic capacitors are recommended for bulk.
2. X5R, X7R, or COG are recommended for ceramics.
3. Place all capacitors as close to associated pins as possible to minimize inductance.

Table 1. Bypass Capacitor Recommendations

Voltage Plane	Pins	Package	C(uf)	Quantity	Comments
3.3 V	VCC33	1210	22	3	
3.3 V	VCC33	603	0.1	12	
3.3 V	VCC33	7343	150	1	
3.3/5.0 V	P_VIO, S_VIO	1210	22	1	See note (1) below
3.3/5.0 V	P_VIO, S_VIO	603	0.1	4	See note (1) below
1.3 V	VCC	1210	22	3	
		603	0.1	12	
1.5 V	VCCA	–	–	–	Filter as described in the *Intel® 31154 133 MHz Bridge Datasheet* (order number 278821).

1. Separate capacitor required only when P_VIO and S_VIO are **not** connected to VCC33.

3.0 Checklists

This section contains two checklists:

- Table 2, “Signals Connection Checklist” on page 7
- Table 3, “Design Checklist” on page 17

Table 2. Signals Connection Checklist (Sheet 1 of 11)

Pin Location	Signals	Recommendations	Comments	Compliance	
				Yes ✓	No ✓
PCI Reset					
E22	P_RST#	Connect to bus RST# signal on primary PCI bus.			
U23	S_RST#	Connect directly to the RST# input pin of all the secondary PCI devices.			
Primary PCI Bus Signals					
B13, C13, B14, C15, A19, B16, C16, A20, B17, C17, C19, D18, F22, F20, G22, B20, G21, H22, H21, J22, J21, K22, D23, K21, E23, K20, G23, L22, L21, M22, M21, J23	P_AD[31:0]	Connect to the primary PCI bus AD[31:0] lines.			
L1, J1, J2, H1, G1, J3, E1, H2, H3, G3, F2, B1, F3, E3, F4, D2, C2, B5, B6, D6, B7, C7, B3, B8, A3, B9, C9, B10, A4, C10, D10, B11	P_AD[63:32]	For 64-bit primary PCI Bus: • Connect to the primary PCI bus AD[63:32]. For 32-bit primary PCI Bus: • Pull up through individual external resistors.	See Note 2 and Note 3 in Section 2.0, “Implementation Notes” on page 6.		
A13, B18, D14, A15	P_CBE[3:0]#	Connect to the primary PCI bus CBE[3:0]#.			

Table 2. Signals Connection Checklist (Sheet 2 of 11)

Pin Location	Signals	Recommendations	Comments	Compliance	
				Yes ✓	No ✓
A5, C11, B12, A7	P_CBE[7:4]#	For 64-bit primary PCI Bus: • Connect to the primary PCI bus CBE[7:4]#. For 32-bit primary PCI Bus: • Pull up through individual external resistors.	• See Note 2 and Note 3 in Section 2.0, "Implementation Notes" on page 6.		
A17	P_FRAME#	Connect to the primary PCI bus FRAME#.			
D21	P_DEVSEL#	Connect to the primary PCI bus DEVSEL#.			
A16	P_IRDY#	Connect to the primary PCI bus IRDY#.			
B15	P_TRDY#	Connect to the primary PCI bus TRDY#.			
C4	P_STOP#	Connect to the primary PCI bus STOP#.			
C20	P_GNT#	Connect to one of the primary PCI bus PCI bus grant signals.			
B19	P_IDSEL#	Connect to one of the primary PCI bus AD lines or the IDSEL# signal of the PCI Add-in card finger (A26).	• See Section 4.3 of the *Intel® 31154 133 MHz Bridge Design Guide*.		
H5	P_M66EN	Connect to the primary PCI bus M66EN signal of the PCI Add-in card finger (B49).			
C18	P_PAR	Connect to the primary PCI bus PAR.			
A9	P_PAR64	Connect to the primary PCI bus PAR64.			
C8	P_PERR#	Connect to the primary PCI bus PERR#.			
B21	P_REQ#	Connect to one of the primary PCI bus PCI bus request signals.			
C12	P_REQ64#	Connect to the primary PCI bus REQ64#.			
B4	P_SERR#	Connect to the primary PCI bus SERR#.			
PCI Bus Interface Clocks					
E21	P_CLK	Connect to the PCI clock on the primary PCI bus.			
P18	S_BRGCLKO	• When the 31154 internal clock is used, connect to S_CLKI through a 33.2 Ω series resistor. • When an external clock is used, NC for this pin.	• All S_CLKO[8:0] and S_BRGCLKO must match in length.		

Table 2. Signals Connection Checklist (Sheet 3 of 11)

Pin Location	Signals	Recommendations	Comments	Compliance	
				Yes ✓	No ✓
J18, K18, J19, K19, M19, L19, N19, P19, R19	S_CLKO[8:0]	• When the 31154 internal clock is used, connect to the secondary PCI devices' PCI clock input through a 33.2 Ω series resistor. • Each clock can be connected to only one PCI device. **Note:** These clocks can be disabled by strapping the S_CLKOEN[3:0] during reset.	• All S_CLKO[8:0] and S_BRGCLKO must match in length. • When a mix of on-board PCI devices and PCI slots is in the design, the 2.5-inch trace length from connector to PCI device on a PCI add-in card must be taken into consideration when determining the matching length. • For asynchronous mode there is no maximum skew between P_CLK and S_CLKI.		
AB23	S_CLKI	• When the 31154 internal clock is used, connect to S_BRGCLKO. • When an external clock is used, connect to the external clock source.	• When using an internal clock, refer to S_BRGCLKO. • When using an external clock source, all secondary clocks must have matching length. • When PCI slots are in the design, S_BRGCLKO must be 3 inches longer to compensate for the 2.5-inch trace length from the connector to PCI device on a PCI add-in card.		
W3	S_CLKSTABLE	• When the 31154 internal clock is used, tie high to 3.3 V through external 8.2 KΩ resistor. • When an external clock source is used, connect to logic that outputs high after the secondary clocks are stable.			
U19	S_GCLKOEN	• When the 31154 internal clock is used, pull up to 3.3 V through external 8.2 KΩ resistor. • When an external clock source is used, tie to GND through 330 Ω external resistor. All secondary clock outputs (S_CLKO[8:0] and S_BRGCLKO) asynchronously tristate.	• When an external clock source is used, tie S_CLKOEN[3:0] to any stable value. Refer to S_CLKOEN[3:0].		

Table 2. Signals Connection Checklist (Sheet 4 of 11)

Pin Location	Signals	Recommendations	Comments	Compliance	
				Yes ✓	No ✓
G2, E2, D1, C6	S_CLKOEN[3:0]	These are strapping pins to enable or tristate S_CLKO[8:0] after reset. • To enable all S_CLKO[8:0] pins, pull all S_CLKOEN[3:0] pins to 3.3 V through an external 8.2 KΩ resistor. • To selectively disable some of the S_CLKO[8:0] pins, refer to the 31154 Control Register 2, bit[8:0].	• This strapping is meaningful only when S_GCLKOEN is pulled high. • When external clocks are used, tie S_GCLKOEN low and tie S_CLKOEN[3:0] to any stable value (0000b for example).		
Hot Swap					
E9	HS_ENUM#	**For hotswap:** Connect to the interrupt input pin to the host. **Not using hotswap:** NC. There is a weak internal pull-up.			
E8	HS_LSTAT	**For hotswap:** Connect to cPCI ejector switch. **Not using hotswap:** Tied low to GND.			
E7	HS_LED_OUT	**For hotswap:** Connect to cPCI blue LED. **Not using hotswap:** NC			
G5	HS_SM	**For hotswap:** Depending on application: • 0 = The 31154 retries any Type 0 Configuration cycles addressed to it until serial ROM preload has completed. **(Default)** • 1 = The 31154 ignores (causes master abort) any Type 0 configuration cycles addressed to it until its serial ROM preload has completed. **Not using hotswap:** Tied low to GND.	• 0 = Tie low to GND. • 1 = Pull up to 3.3 V through an external 8.2 KΩ resistor.		
E12, E13	HS_FREQ[1:0]	**For hotswap:** Depending on the primary PCI bus frequency: • 00 = PCI Mode, 33 or 66 MHz **(Default)** • 01 = PCI-X 66 MHz • 10 = PCI-X 100 MHz • 11 = PCI-X 133 MHz **Not using hotswap:** Tied low to GND.	• Valid only when HS_SM = 1. • 0 = Tie low to GND. • 1 = Pull up to 3.3 V through an external 8.2 KΩ resistor.		

Table 2. Signals Connection Checklist (Sheet 5 of 11)

Pin Location	Signals	Recommendations	Comments	Compliance	
				Yes ✓	No ✓
Hardware Straps		Hardware strapping pins are sampled at the trailing edge of P_RST#.			
T21	S_ARB_DISABLE/ S_ARB_LOCK	S_ARB_DISABLE (sampled on the trailing edge of P_RST#): • To disable the internal secondary arbiter: - Pull up to 3.3 V through an external 8.2 KΩ resistor. - S_GNT0# becomes the 31154 secondary PCI bus request output, and S_REQ0# becomes the 31154 secondary PCI bus grant input. • To enable internal secondary arbiter: - Pull down to GND through an external 220 Ω resistor. **(Default)** S_ARB_LOCK (After trailing edge of P_RST#): • Sampled as 1b, the 31154 internal secondary bus arbiter locks and provides the grant only to itself. **Note:** S_ARB_LOCK has an effect only when the internal arbiter is enabled.	When an internal arbiter is used and 1b is sampled after the trailing edge of P_RST#, the 31154 internal secondary bus arbiter locks and provides grant only to itself.		
V3	S_MAX100	• To limit secondary bus frequency to maximum of 100 MHz: - Pull up to 3.3 V through an external 8.2 KΩ resistor. • To allow secondary bus frequency to exceed 100 MHz: - Pull down to GND through an external 330 Ω resistor. **(Default)**			
AA18	OPAQUE_EN	• To enable Opaque Memory Base/Limit Registers to establish private memory space for secondary bus usage: - Pull up through 3.3 V through an external 8.2 KΩ resistor. • To disable Opaque Memory Base/Limit Registers: - Pull down to GND through an external 220 Ω resistor. **(Default)**			
AC22	IDSEL_MASK	• To enable device hiding after reset (that is, hide devices number 16–21 from the host): - Pull up to 3.3 V through an external 8.2 KΩ resistor. • To disable device hiding after reset: - Pull down to GND through external 220 Ω resistor. **(Default)**	After reset, device hiding can be done through software through the Secondary IDSEL Select Register (Offset 5Ch).		

Table 2. Signals Connection Checklist (Sheet 6 of 11)

Pin Location	Signals	Recommendations	Comments	Compliance	
				Yes ✓	No ✓
Y22	DEV_64BIT#	This bit is used by system management software to help the user identify the best slot for an add-in card: • When the 31154 is installed on an add-in card, and the add-in card implements a 64-bit PCI connector, pull up to 3.3 V through an external 8.2 KΩ resistor. • When the 31154 is not installed on an add-in card, or the add-in card implements only a 32-bit PCI connector, pull down to GND through an external 220 Ω resistor. **(Default)**			
Serial EEPROM		The 31154 supports glueless interface to an optional 512-Byte serial EEPROM, such as Microwire* Serial ROM by Microchip Technology, Inc., 93LC66A 512x8 serial EEPROM.			
J5	SR_CLK	Serial ROM clock input: • Connect to the clock input of the EEPROM. • NC when EEPROM is not required in design.			
N5	SR_DI	Serial ROM data input: • Connect to the DI input of the EEPROM. • NC when EEPROM is not required in design.			
M5	SR_DO	Serial ROM data output: • Connect to the DO output of the EEPROM. • Tie high or pull down to GND when EEPROM is not required in design.	When an EEPROM is present but register preload is not desired, bit[7:6] of the first byte can be any value except the preload enable value (10b).		
L5	SR_CS	Serial ROM chip select: • Connect to the Chip Select of the EEPROM. • NC when EEPROM is not required in design.			
JTAG					
F21	TCK	Pull down to GND when not used. See the *Intel® 31154 133 MHz Bridge Design Guide* (278944) and the *Intel® 31154 133 MHz Bridge Specification Update* (300826) for details.			
C22	TDI	Pull up to 3.3 V through an external 8.2 KΩ resistor when not used.			
B23	TDO	NC when not used.			
C23	TRST#	Pull down to GND through an external 1 KΩ resistor when not used.			
D22	TMS	Pull up to 3.3 V through an external 8.2 KΩ resistor when not used.			

Table 2. Signals Connection Checklist (Sheet 7 of 11)

Pin Location	Signals	Recommendations	Comments	Compliance	
				Yes ✓	No ✓
Power					
AB21	S_VCCA	Connect to 1.3 V supply through a low-pass filter to reduce noise-induced jitter. The 4.7 µF capacitor must be low-ESR solid tantalum; the 0.01 µF capacitor must be of type X7R; and the node connecting VCCPLL must be as short as possible.	• Ensure that the voltage at the input pin is within S_VCCA min./max. range. • For power sequencing, see chapter 6 of the *Intel® 31154 133 MHz Bridge Design Guide* (278944).		
A21	P_VCCA	Connect to 1.3 V supply through a low-pass filter to reduce noise-induced jitter. The 4.7 µF capacitor must be low-ESR solid tantalum; the 0.01 µF capacitor must be of type X7R; and the node connecting VCCPLL must be as short as possible.	• Ensure that the voltage at the input pin is within P_VCCA min./max. range. • For power sequencing, see chapter 6 of the *Intel® 31154 133 MHz Bridge Design Guide* (278944).		
D9, D11, D13, D15, F6, F8, F10, F15, F17, G18, H6, H19, J4, J20, K6, L4, L20, N4, N20, R4, R20, R6, T18, T19, U6, V7, V9, V14, V18, W13, Y9, Y11, Y13, Y15	VCC	Connect to 1.3 V supply.			
A8, A12, A22, AC2, AC12, AC16, C5, D5, D7, D17, D19, E4, E20, G4, G20, M1, U4, U20, W4, W20, Y5, Y7, Y17, Y19	VCCP	Connect to 3.3 V supply.			

Table 2. Signals Connection Checklist (Sheet 8 of 11)

Pin Location	Signals	Recommendations	Comments	Compliance	
				Yes ✓	No ✓
H23	PVIO	Connect to 5 V or 3.3 V power supply. There is power sequence requirement when P_VIO is not connected to the same power supply as VCCP. Please refer to Note 4 in Section 2.0, "Implementation Notes" on page 6.			
T1	SVIO	Connect to 5 V or 3.3 V power supply. There is power sequence requirement when S_VIOS is not connected to the same power supply as VCCP. Please refer to Note 4 in Section 2.0, "Implementation Notes" on page 6.			
Miscellaneous					
E5	R_REF	Pull down to GND through an external 30 Ω 1% resistor.			
C14, AC20	MT0# and MT1#	Pull up to 3.3 V through an external 8.2 KΩ series resistor.	**Manufacturing use only.**		
AA22	RSTV0	Tie to GND through a 0 Ω external resistor.			
AC7	RSRV1	Tie to GND through a 0 Ω external resistor.	**Manufacturing use only.**		
R18	S_M66EN	Meaningful only when S_PCIXCAP is connected to GND (that is, secondary PCI bus in legacy PCI mode): • Design without secondary PCI slot: - When the secondary PCI devices (and loading) support 66 MHz PCI bus, pull-up to 3.3 V through a 8.2 KΩ series resistor. - When the secondary PCI devices (and loading) do not support 66 MHz PCI bus, tie this pin to GND. • Design with secondary PCI Slot: - When the onboard PCI devices do not support 66 MHz PCI bus, GND this pin. - When the onboard PCI devices do support 66 MHz PCI bus, connect this pin to M66EN (Pin49B) of the PCI connector.	Refer to the *PCI-X Addendum to the PCI Local Bus Specification*, revision 1.0b, Table 6-1.		

Table 2. Signals Connection Checklist (Sheet 9 of 11)

Pin Location	Signals	Recommendations	Comments	Compliance	
				Yes ✓	No ✓
R23	S_PCIXCAP	• Design without secondary PCI slot: - When there is at least one legacy PCI device on the secondary PCI bus, tie this pin directly to GND. - When there is at least one PCI-X device that supports only maximum PCI-X 66 MHz on the secondary PCI bus, pull down to GND through a 10 KΩ series resistor. - When all secondary PCI-X devices (and the bus loading) support PCI-X 133 MHz, leave this pin unconnected (except for decoupling capacitor). • Design with secondary PCI slot: - When there is at least one on-board legacy PCI device on the secondary PCI bus, tie this pin directly to GND. - Otherwise, pull up to 3.3 V through a 10 KΩ resistor and connect this pin to PCIXCAP (Pin B38) of the PCI connector (assuming bus loading supports up to PCI-X 133 MHz).	Refer to the *PCI-X Addendum to the PCI Local Bus Specification*, revision 1.0b, Table 6-1.		
E15	NT_MASK#	• When forced retirement of the 31154 internal request queues and data buffer is not desired in the application, this pin must be pulled up to 3.3 V through an 8.2 KΩ.resistor. • When forced retirement of the 31154 internal request queues and data buffer is desired in the application, this pin must be connected to external logic (or using the 31154 GPIO) that drives this pin low when masking new transaction is desired.	• When NT_MASK# is asserted, it must not be de-asserted until the QE pin is asserted. • NT_MASK# must not be reasserted until the QE pin is cleared. • Setting New Transaction Mask bit to 1b in VCR0 has the same effect as asserting NT_MASK#.		
D3	QE	Depends on application. This is an output signal that indicates the state of the 31154 internal request and data queues. When at logic level high, this signal indicates that the 31154 internal queues are completely empty. NC when not used.	The state of this output is valid only when the NT_MASK# pin is asserted.		
C1	SCAN_EN	For normal operation, tie low to GND. **(Manufacturing use only.)**			
W22, Y21, AA4, Y23	TMODE[3:0]	For normal operation, tie to 0000 or 0111. **(Manufacturing use only.)**	0 = Pull down to GND. 1 = Pull up to 3.3 V through an external 8.2 KΩ resistor.		

Table 2. Signals Connection Checklist (Sheet 10 of 11)

Pin Location	Signals	Recommendations	Comments	Compliance	
				Yes ✓	No ✓
Pull Up 64-bit extension signals					
K4, K3, K2, L3, L2, R1, M3, M2, N3, N2, U1, P4, W1, P3, Y1, P2, R3, R2, T3, T2, U3, U2, V4, V2, Y3, Y6, AA5, AA6, AB6, AA7, AB7, AB8	S_AD[63:32]	Pull up to 3.3 V through external resistors.	See Note 1 and Note 2 in Section 2.0, "Implementation Notes" on page 6		
AC8, AA11, AB10, Y10	S_CBE[7:4]#	Pull up to 3.3 V through external resistors.	See Note 1 and Note 2 in Section 2.0, "Implementation Notes" on page 6		
AB13	S_REQ64#	Pull up to 3.3 V through external resistors.	See Note 1 and Note 2 in Section 2.0, "Implementation Notes" on page 6		
AA8	S_ACK64#	Pull up to 3.3 V through external resistors.	See Note 1 and Note 2 in Section 2.0, "Implementation Notes" on page 6		
PCI Control Signals					
AA14, AC19, Y14, AB20, AC21, AB17, AB19	S_FRAME#, S_IRDY#, S_TRDY#, S_STOP#, S_DEVSEL#, S_PERR#, S_SERR#,	Pull up to 3.3 V through external resistors.	See Note 1 and Note 2 in Section 2.0, "Implementation Notes" on page 6		

Table 2. Signals Connection Checklist (Sheet 11 of 11)

Pin Location	Signals	Recommendations	Comments	Compliance	
				Yes ✓	No ✓
Secondary REQ#					
AA23, AA2, W2, AB3, AB5, AC3, W5, T5, W15, AA19	S_REQ[8:1]#, S_REQ0#/BR_GNT#, S_GNT0#/BR_REQ#	Pull up to 3.3 V through external resistors when either internal or external arbiter is used.	See Note 1 and Note 2 in Section 2.0, "Implementation Notes" on page 6		
Secondary GNT#					
AB1, Y2, AC5, AB4, AC4, U5, R5, V17	S_GNT1#, S_GNT2#, S_GNT3#, S_GNT4#, S_GNT5#, S_GNT6#, S_GNT7#, S_GNT8#	• Connect to GNT# input of the PCI devices on the secondary PCI bus. • NC when S_GNT# is not used.			

Table 3. Design Checklist

Guideline		Compliance	
		Yes	No
Secondary IDSEL	The 31154 converts a Type 1 configuration access on its primary PCI bus to Type 0 configuration on its secondary PCI bus when necessary.		
Only S_AD[31:17] is used to connect to the IDSEL of the PCI devices on the secondary PCI bus.			
S_AD[31:17] is connected to IDSEL of secondary PCI bus through an external 2 KΩ series coupling resistor for a PCI-X system.			
Power Sequencing			
For power sequencing, see Section 6.2 of the *Intel® 31154 133 MHz Bridge Design Guide* (278944).			
Secondary REQ# and GNT# – Internal secondary arbiter is used			
S_REQ[8:1]#, S_REQ0#/BR_GNT# and S_GNT0#/BR_REQ# are pulled up to secondary VIO voltage through external 8.2 KΩ resistors.			
Secondary REQ# and GNT# – External secondary arbiter is used			
S_REQ0#/BR_GNT# is connected to external arbiter's GNT# output pin.			
S_GNT0#/BR_REQ# is connected to external arbiter's REQ# input pin.			

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